

FIG. 1A
SEM PHOTOGRAPH (CROSS SECTION)

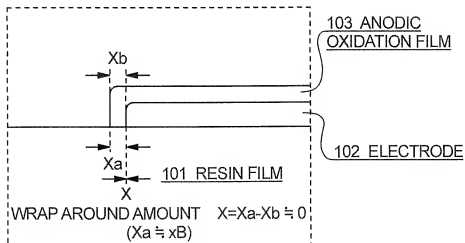


FIG. 1B
SCHEMATIC DIAGRAM OF ENLARGED ELECTRODE EDGE PORTION

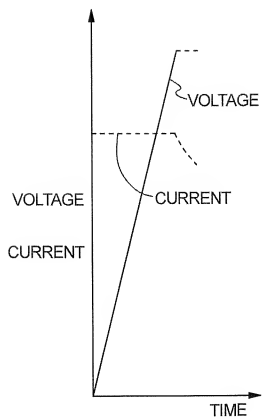


FIG. 2

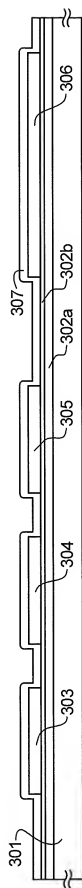


FIG. 3A

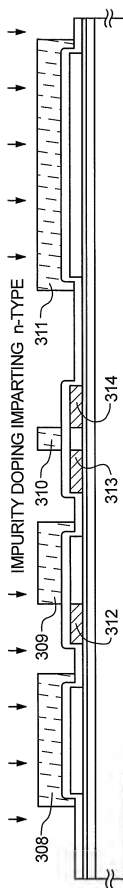


FIG. 3B

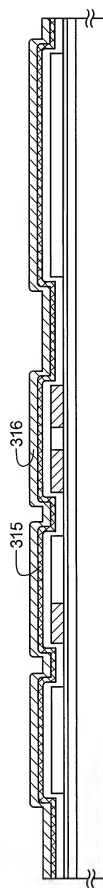


FIG. 3C

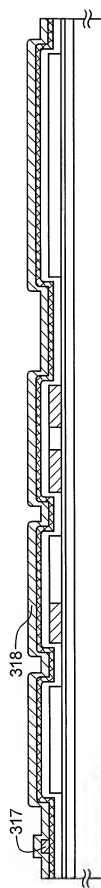


FIG. 3D

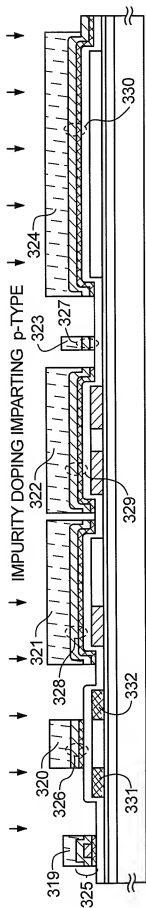
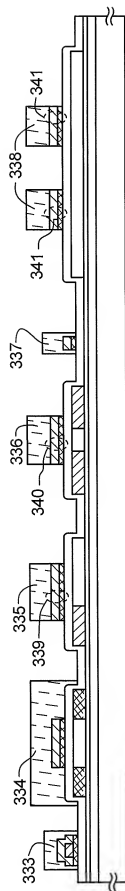
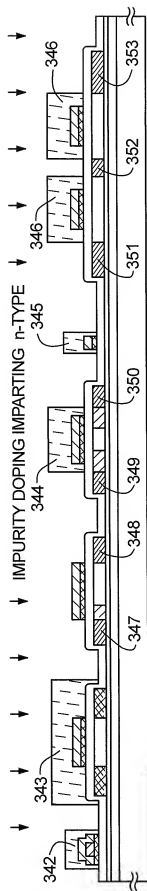
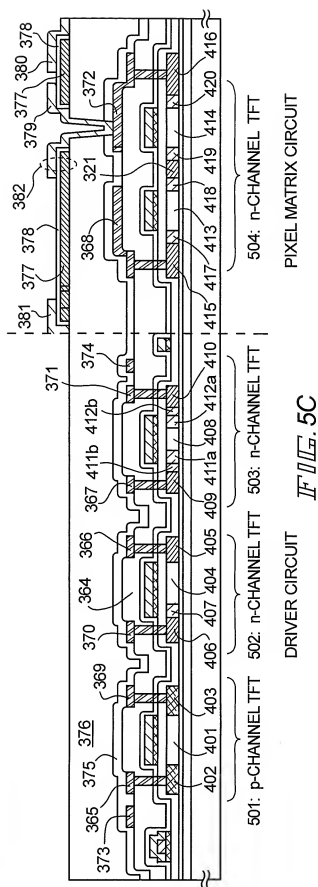
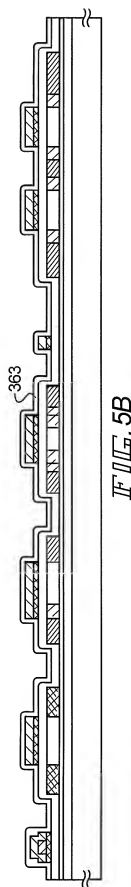
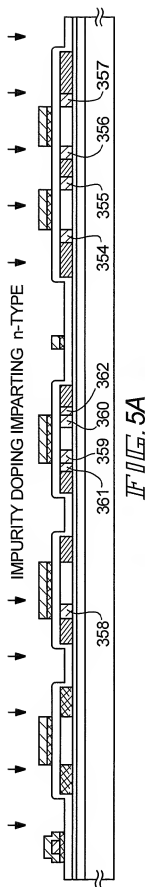
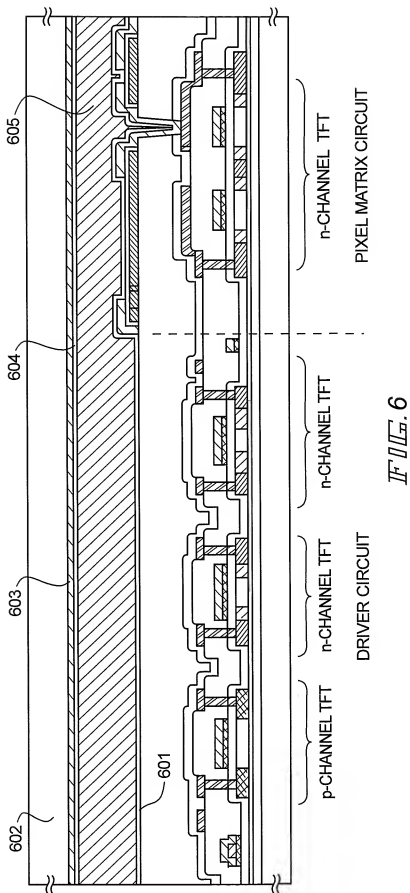


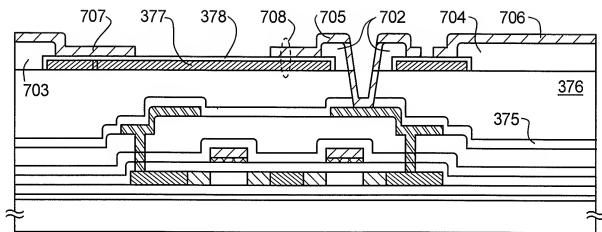
FIG. 4A


$$F[\mathbb{G}, 4B]$$


FILE. 4C







701: n-CHANNEL TFT

FIG. 7

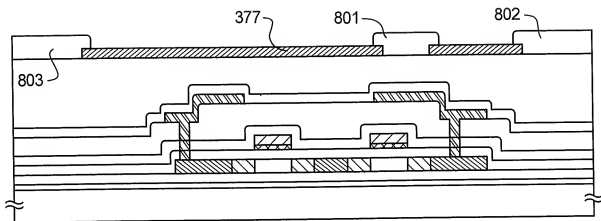


FIG. 8A

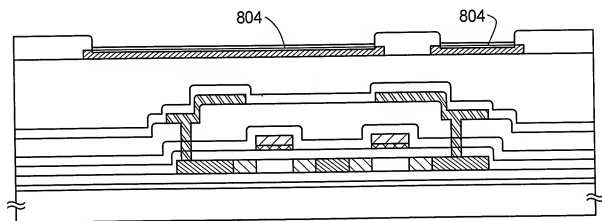


FIG. 8B

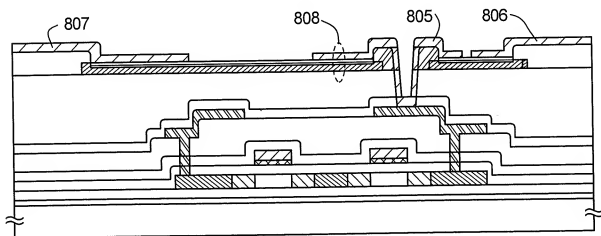
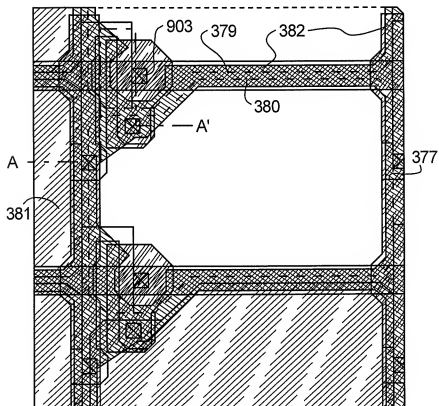
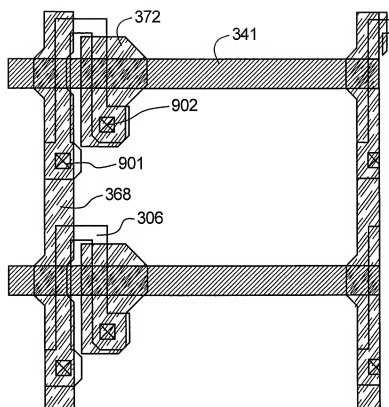


FIG. 8C



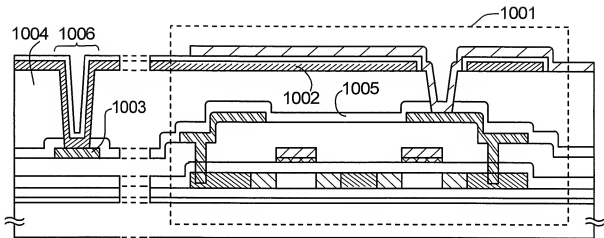


FIG. 10A

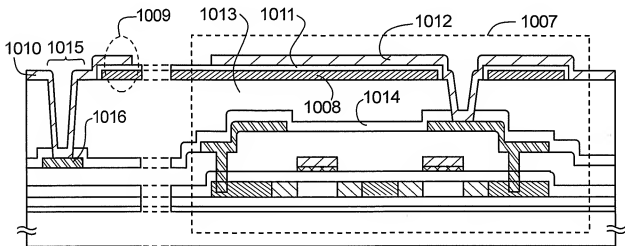


FIG. 10B

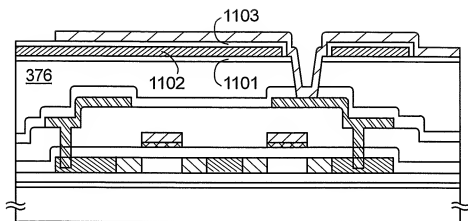


FIG. 11A

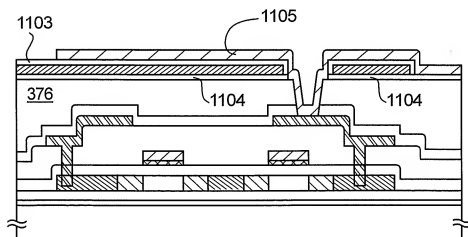
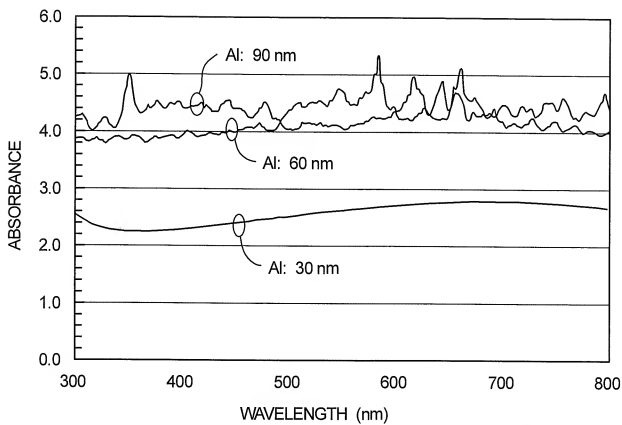


FIG. 11B

*FIG. 12*

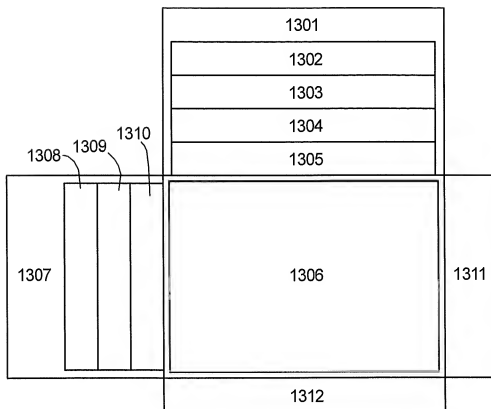


FIG. 13

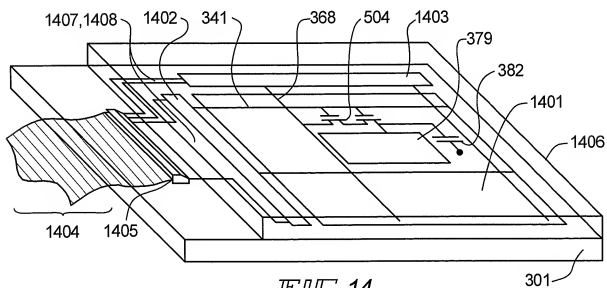


FIG. 14

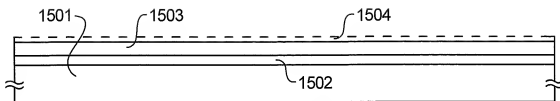


FIG. 15A

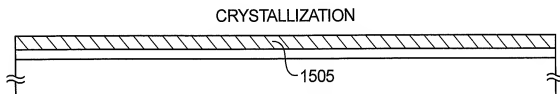


FIG. 15B

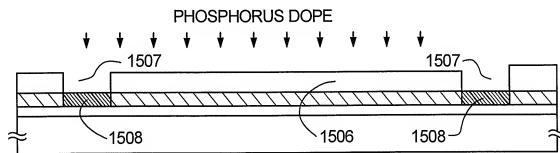


FIG. 15C

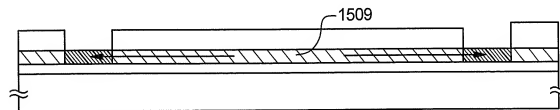


FIG. 15D

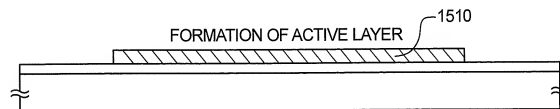


FIG. 15E

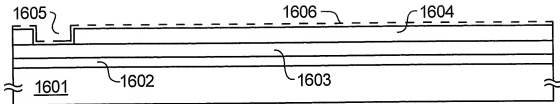


FIG. 16A

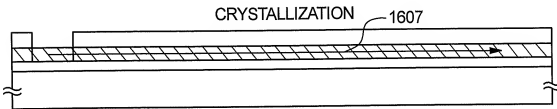


FIG. 16B

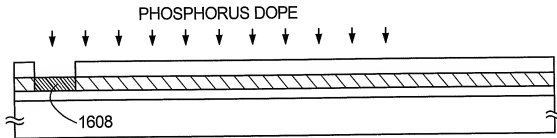


FIG. 16C

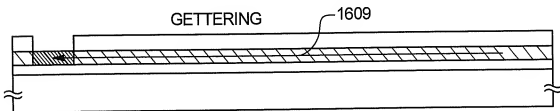


FIG. 16D

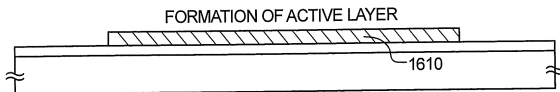
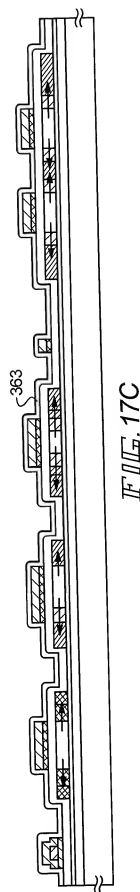
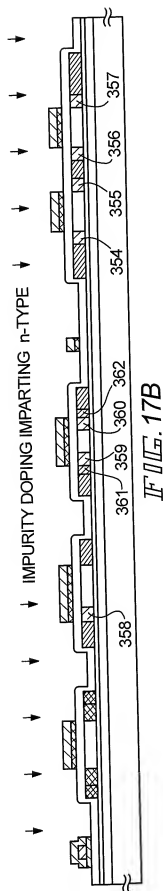
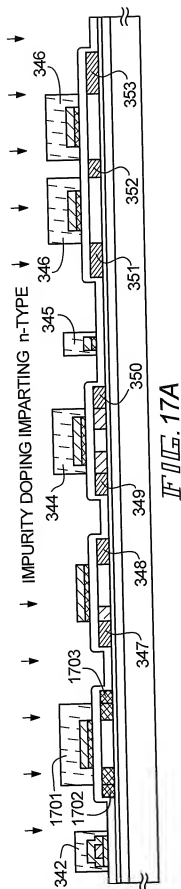


FIG. 16E



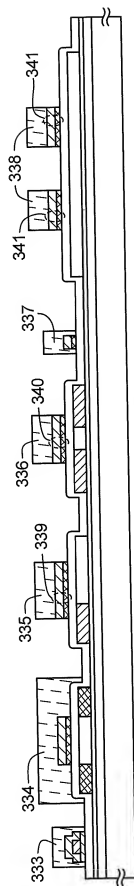


FIG. 18A

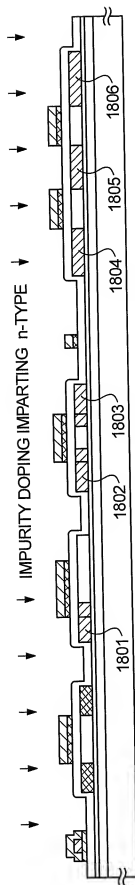


FIG. 18B FORMING n - - REGION

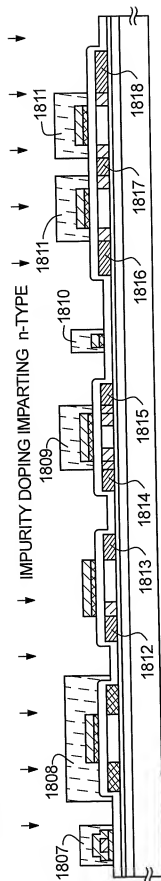


FIG. 18C FORMING n + REGION

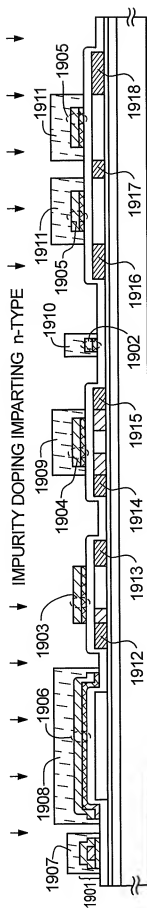


FIG. 19A FORMING n+ REGION

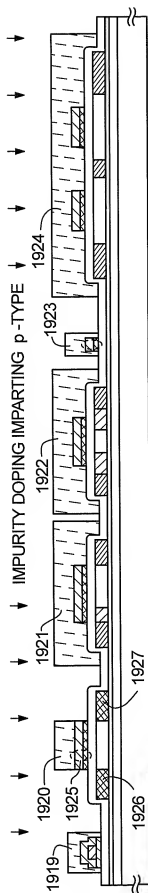


FIG. 19B FORMING p-ch TFT GATE WIRING, FORMING p++ REGION

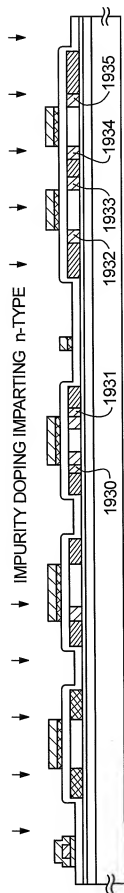


FIG. 19C FORMING n-- REGION

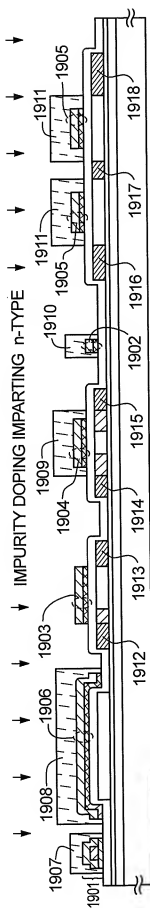


FIG. 20A FORMING n+ REGION

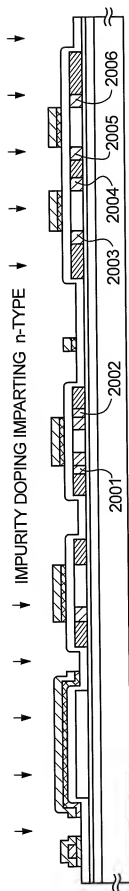


FIG. 20B FORMING n-- REGION

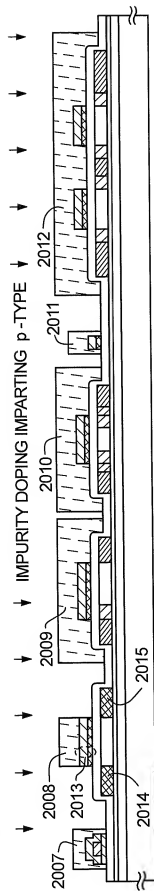


FIG. 20C FORMING p-ch TFT GATE WIRING, FORMING p++ REGION

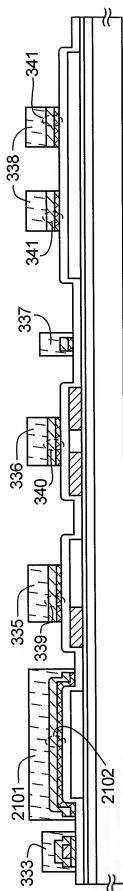


FIG. 21A FORMING n-ch TFT GATE WIRING

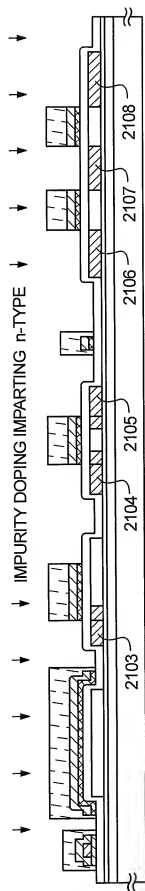


FIG. 21B FORMING n-- REGION

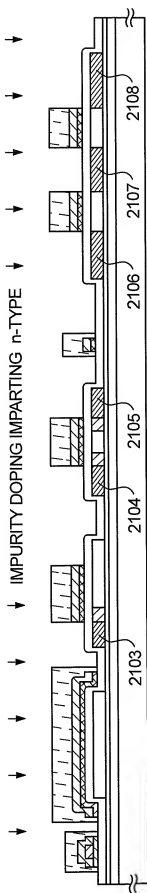


FIG. 22A FORMING n-- REGION

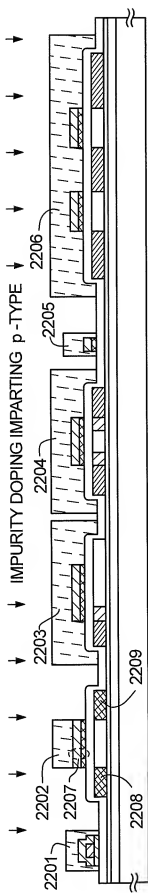


FIG. 22B FORMING p-ch TFT GATE WIRING, FORMING p++ REGION

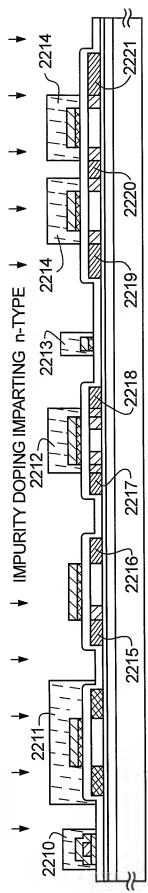


FIG. 22C FORMING n+ REGION

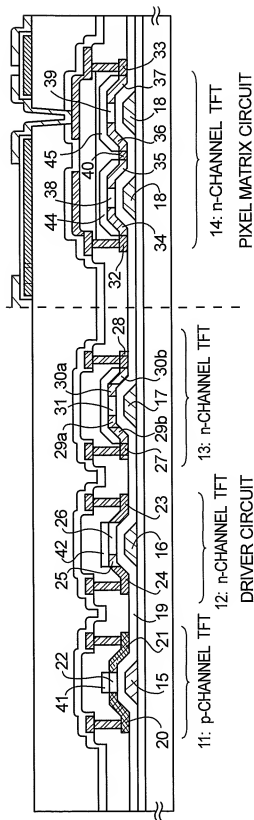


FIG. 23

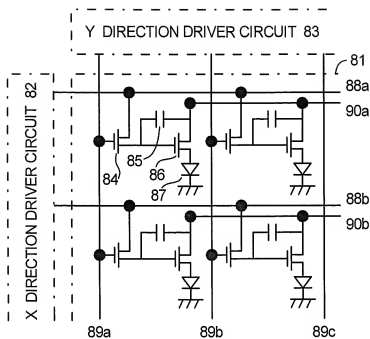


FIG. 24A EL PANEL CIRCUIT DIAGRAM

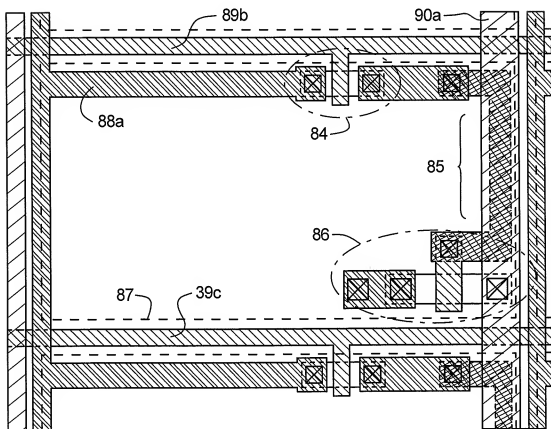


FIG. 24B TOP VIEW OF EL PANEL PIXEL SECTION

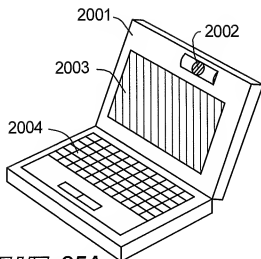


FIG. 25A

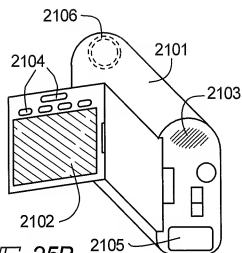


FIG. 25B

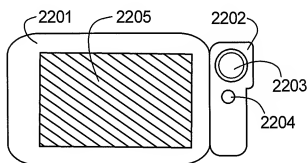


FIG. 25C

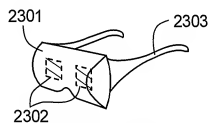


FIG. 25D

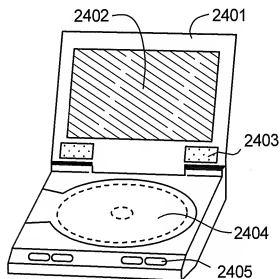


FIG. 25E

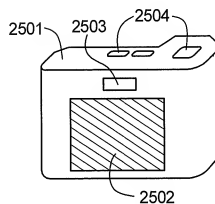


FIG. 25F

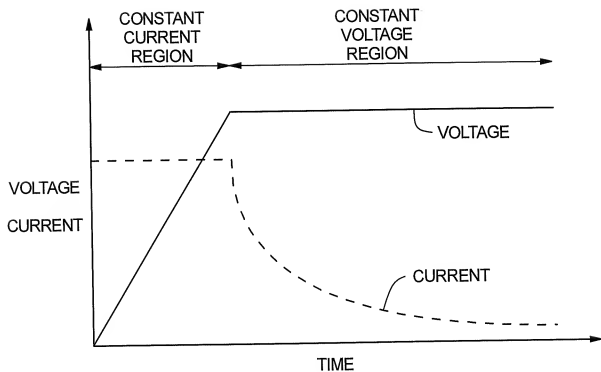
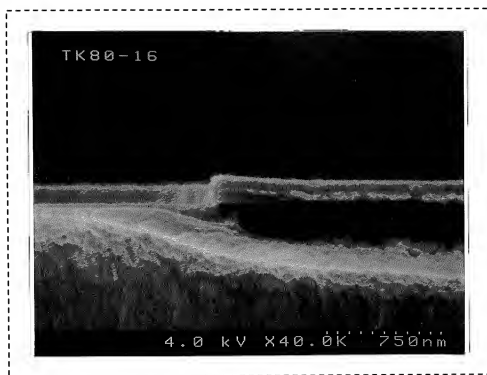


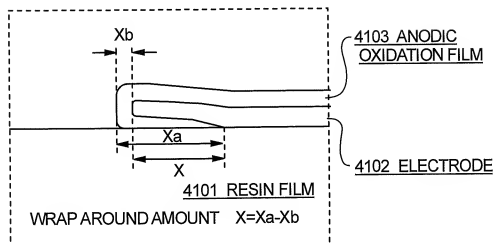
DIAGRAM SHOWING THE RELATIONSHIP BETWEEN VOLTAGE
AND ELECTRIC CURRENT BETWEEN THE ELECTRODES IN A
CONVENTIONAL ANODIC OXIDATION PROCESS

FIG. 26
PRIOR ART



SEM PHOTOGRAPH (CROSS SECTION)

FIG. 27A
PRIOR ART



SCHEMATIC DIAGRAM OF ENLARGED ELECTRODE EDGE PORTION

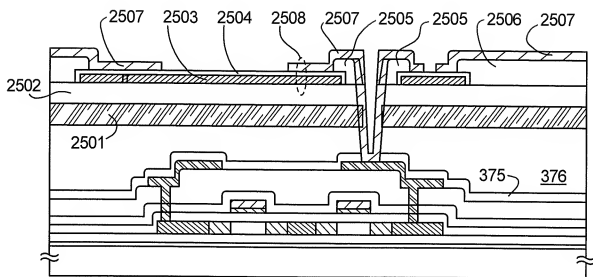
FIG. 27B
PRIOR ART



FIG. 28A

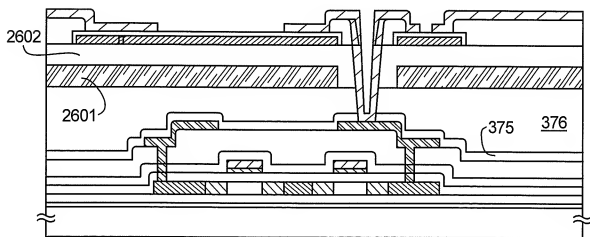


FIG. 28B



701: n-CHANNEL TFT

FIG. 29A



701: n-CHANNEL TFT

FIG. 29B



SEM PHOTOGRAPH (CROSS SECTION)

FIG. 30A

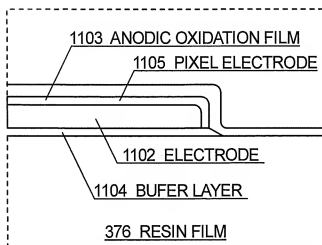
SCHEMATIC DIAGRAM OF ENLARGED
ELECTRODE EDGE PORTION

FIG. 30B

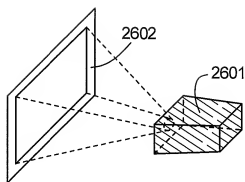


FIG. 31A

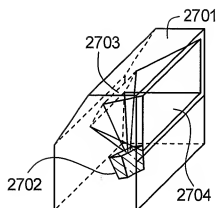
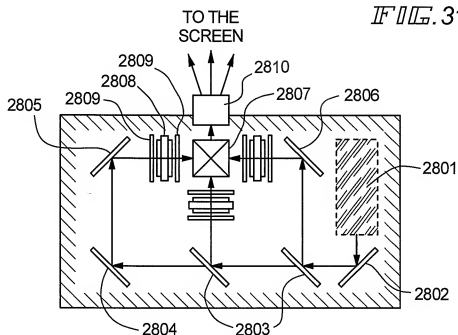
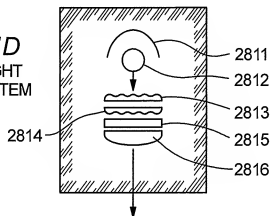


FIG. 31B



PROJECTION DEVICE (THREE PLATE TYPE)

FIG. 31C

FIG. 31D
OPTICAL LIGHT
SOURCE SYSTEM

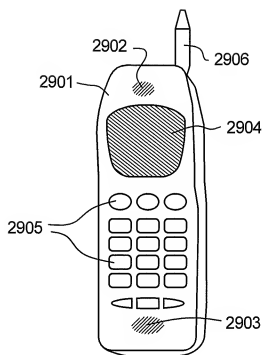


FIG. 32A

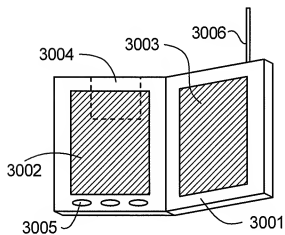


FIG. 32B

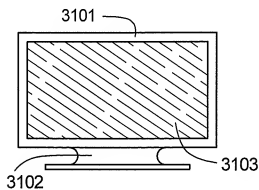


FIG. 32C

